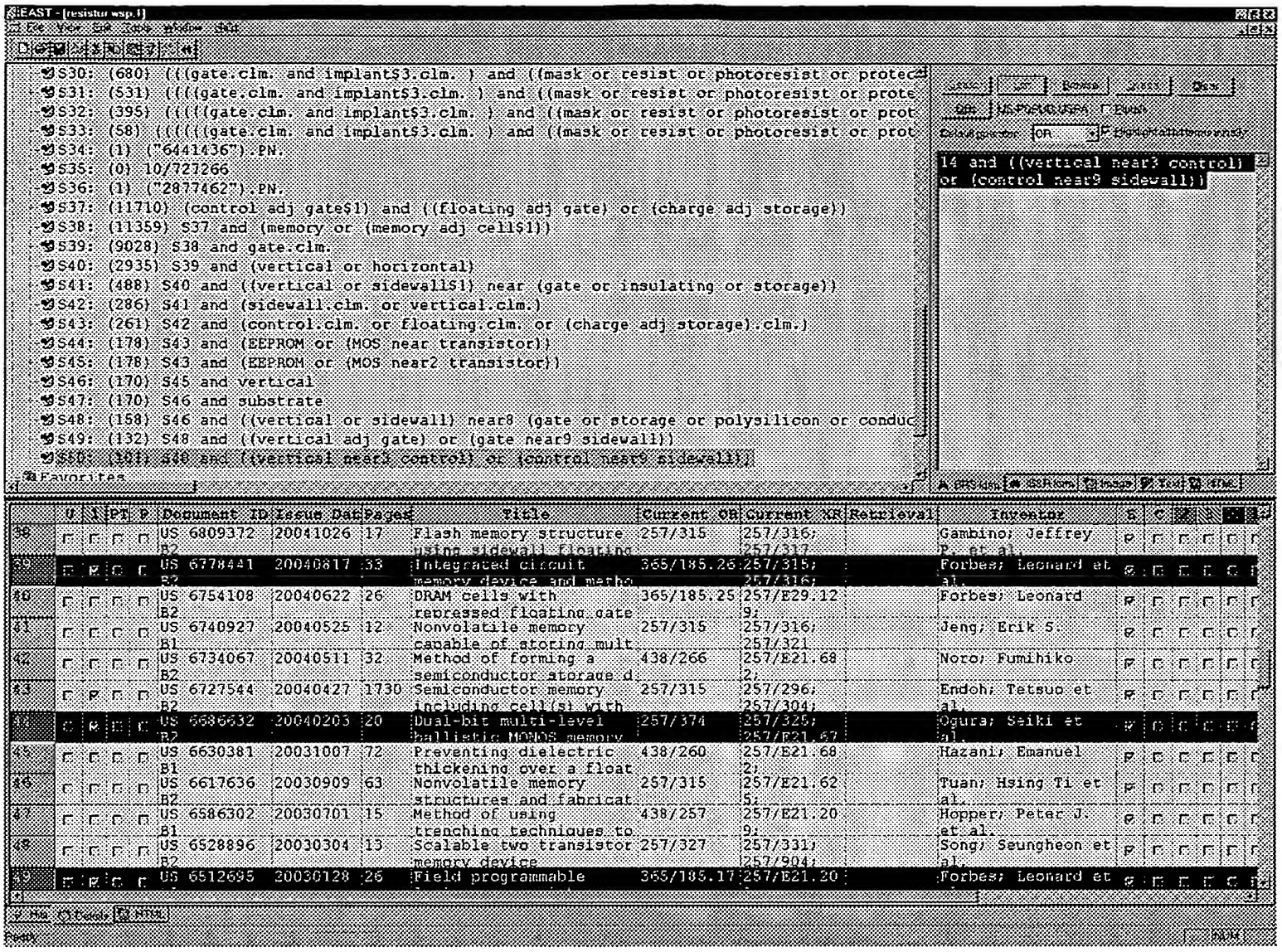
EAST - [resistor wsp.1]
File View Edit Tools Window Help
S30: (680) (((gate.clm. and implant$3.clm.) and ((mask or resist or photoresist or protec
S31: (531) ((((gate.clm. and implant$3.clm.) and ((mask or resist or photoresist or prote
S32: (395) (((((gate.clm. and implant$3.clm.) and ((mask or resist or photoresist or prot
S33: (58) ((((((gate.clm. and implant$3.clm.) and ((mask or resist or photoresist or prot
S34: (1) ("6441436").PN.
S35: (0) 10/727266
S36: (1) ("2877462").PN.
S37: (11710) (control adj gate$1) and ((floating adj gate) or (charge adj storage))
S38: (11359) S37 and (memory or (memory adj cell$1))
S39: (9028) S38 and gate.clm.
S40: (2935) S39 and (vertical or horizontal)
S41: (408) S40 and ((vertical or sidewall$1) near (gate or insulating or storage))
S42: (286) S41 and (sidewall.clm. or vertical.clm.)
S43: (261) S42 and (control.clm. or floating.clm. or (charge adj storage).clm.)
S44: (178) S43 and (EEPROM or (MOS near transistor))
S45: (178) S43 and (EEPROM or (MOS near2 transistor))
S46: (170) S45 and vertical
S47: (170) S46 and substrate
S48: (158) S46 and ((vertical or sidewall) near8 (gate or storage or polysilicon or conduc
S49: (132) S48 and ((vertical adj gate) or (gate near9 sidewall))
S50: (101) S48 and ((vertical near3 control) or (control near9 sidewall))
14 and ((vertical near3 control) or (control near9 sidewall))
Favorites
Document ID
Issue Dat
Page
Title
Current OR
Current XR
Retrieval
Inventor
38 US 6809372 B2 20041026 17 Flash memory structure using sidewall floating ... 257/315 257/316; 257/317 Gambino; Jeffrey P. et al.
39 US 6778441 B2 20040817 33 Integrated circuit memory device and metho... 365/185.26 257/315; 257/316; Forbes; Leonard et al.
40 US 6754108 B2 20040622 26 DRAM cells with repressed floating gate ... 365/185.25 257/E29.129; Forbes; Leonard
41 US 6740927 B1 20040525 12 Nonvolatile memory capable of storing mult... 257/315 257/316; 257/321 Jeng; Erik S.
42 US 6734067 B2 20040511 32 Method of forming a semiconductor storage d... 438/266 257/E21.682; Noro; Fumihiko
43 US 6727544 B2 20040427 1730 Semiconductor memory including cell(s) with ... 257/315 257/296; 257/304; Endoh; Tetsuo et al.
44 US 6686632 B2 20040203 20 Dual-bit multi-level ballistic MONOS memory ... 257/374 257/325; 257/E21.67 Ogura; Seiki et al.
45 US 6630381 B1 20031007 72 Preventing dielectric thickening over a float... 438/260 257/E21.682; Hazani; Emanuel
46 US 6617636 B2 20030909 63 Nonvolatile memory structures and fabricat... 257/315 257/E21.625; Tuan; Hsing Ti et al.
47 US 6586302 B1 20030701 15 Method of using trenching techniques to ... 438/257 257/E21.209; Hopper; Peter J. et al.
48 US 6528896 B2 20030304 13 Scalable two transistor memory device ... 257/327 257/331; 257/904; Song; Seungheon et al.
49 US 6512695 20030128 26 Field programmable 365/185.17 257/E21.20 Forbes; Leonard et
Text
HTML
Path
NUM